

## Patent Abstracts of Japan

PUBLICATION NUMBER : 04137816  
PUBLICATION DATE : 12-05-92

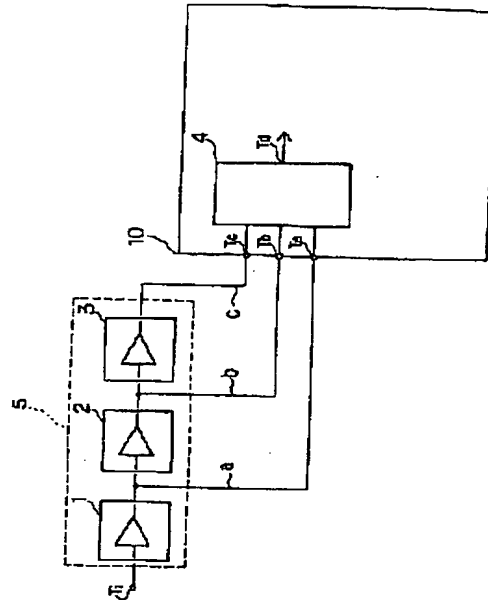
APPLICATION DATE : 28-09-90  
APPLICATION NUMBER : 02257199

APPLICANT : NEC MIYAGI LTD;

INVENTOR : SHIMAMORI TETSUYA;

INT.CL. : H03K 5/01

TITLE : NOISE ELIMINATING CIRCUIT



**ABSTRACT :** PURPOSE: To eliminate the deformation of a waveform and a change in the duty cycle by using a delay circuit so as to form three or more output signals and taking majority decision over them so as to eliminate noise.

CONSTITUTION: This circuit is provided with a 1st delay circuit 1 delaying a clock signal inputted from an input terminal Ti by a prescribed time, a 2nd delay circuit 2 delaying an output from the 1st delay circuit 1 by a prescribed time and a 3rd delay circuit 3 delaying an output from the 1st delay circuit 1 by a prescribed time and a majority decision circuit 4 fetching the three output signals from the delay circuits 1-3 and taking logical majority decision. Then a clock signal (d) from which the noise is eliminated is obtained from the output terminal Td of the majority decision circuit 4. Thus, the circuit is constituted of a digital component and the noise is eliminated without unsharpening the waveform and deteriorating the duty factor.

COPYRIGHT: (C)1992,JPO&Japio